REMARKS

In response to the non-final Office Action mailed May 21, 2008, Applicant respectfully requests reconsideration. Claims 1, 3-15 and 17-23 were previously pending in this application. By this amendment, claims 1 and 14 have been amended. No claims have been canceled and no claims have been added. As a result, claims 1, 3-15 and 17-23 are pending for examination with claims 1 and 14 being independent.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 1, 3-5, 7, 10, 12-15, 17, 18 and 21 under 35 U.S.C. §103(a) as purportedly being unpatentable over Mahalingaiah (US Patent No. 5,960,467) in view of Gandhi (U.S. Patent No. 6,405,305) and in further view of Meier (US Patent No. 6,405,305). Applicant respectfully traverses this rejection. Applicant appreciates the Examiner's clear indication of how the claims are being interpreted in the Response to Arguments section of the Office Action. In particular, the Examiner indicated that the limitations of the claims, as presented, can be met by selecting any plural number of stages in the pipelines disclosed in the alleged combination. While Applicant does not agree that, even under this interpretation, the alleged combination discloses each of the limitations of the claims as previously presented, Applicant has amended each of the independent claims to require that the pipeline include each of a plural number of pipeline stages required to execute instructions from an initial stage in which instructions are fetched through a final stage during which the instructions are completed." That is, the plural number of stages include each stage in the pipeline, however implemented.

As discussed in a previous response, some embodiments of Applicant's invention address the problem of excess power consumption in conventional instruction pipeline architecture resulting from reading/writing architectural data addresses between multiple register structures, which may occur on every clock cycle (*see e.g.*, Page 2, final paragraph of the specification). To conserve at least some of the power used in reading/writing architectural data addresses between different register structures, Applicant proposes increasing the size of the speculative register file such that it is capable of holding a number of speculative data addresses equal to or greater than the number of stages in the *entire* pipeline, and capable of holding at least one additional architectural data address.

Accordingly, arbitrarily choosing any plural number of stages is not sufficient to meet the limitations of the claims, as amended, as the claims require that the plural number of stages include *each* stage in the pipeline required to execute instructions from an initial stage in which the instructions are fetched through a final stage in which the instructions are completed. With the requirement that the plural number of stages include each stage in the pipeline needed to execute the instructions, the alleged combination nowhere discloses or suggests a speculative register file capable of simultaneously storing at least a number of speculative data addresses equal to or greater than the plural number of pipeline stages and at least one architectural address. That is, when each stage in an instruction pipeline required to complete the execution of an instruction is included, nowhere does the alleged combination disclose or suggest a speculative register file capable of storing the number of data addresses recited in the claims.

A. Claims 1 and 3-13

Claim 1, as amended, recites, *inter alia*, "a pipelined execution unit configured to execute instructions in an instruction pipeline including each of a plural number of stages required to execute instructions from an initial stage in which instructions are fetched through a final stage in which execution of the instructions are completed, the plural number of stages using data at locations specified by the speculative data addresses." Having thus defined the instruction pipeline, the alleged combination of Mahalingaiah, Gandhi and Meier does not disclose or suggest a digital signal processor having "a speculative register file capable of simultaneously storing *at least a number of speculative data addresses equal to or greater than the plural number of pipeline stages and at least one architectural data address*, the speculative register file configured to hold the speculative data addresses as corresponding instructions advance through the instruction pipeline and at least one speculative data address after the at least one speculative data address becomes a respective architectural data address," as recited in claim 1 (emphasis added). Therefore, claim 1 patentably distinguishes over the alleged combination and is in allowable condition.

Claims 3-13 depend from claim 1 and are allowable based at least on their dependency.

B. Claims 14, 15 and 17-23

Claim 14, as amended, recites, *inter alia*, "executing an instruction using data at a location specified by the speculative data addresses in a pipelined execution unit including each

of a plural number of pipeline stages required to execute the instruction from an initial stage in which the instruction is fetched through a final stage in which execution of the instruction is completed." Having thus defined the executing act, the alleged combination of Mahalingaiah, Gandhi and Meier nowhere discloses or suggests holding speculative data addresses in a speculative register file as a corresponding instruction advances through the pipeline, "the speculative register file capable of storing *a number of speculative data addresses equal to or greater than the plural number of pipeline stages in the pipelined execution unit and at least one architectural data address*," as recited in claim 14 (emphasis added). Therefore, claim 14 patentably distinguishes over the combination and is in allowable condition. Claims 15 and 17-23 depend from claim 14 and are allowable based at least on their dependency.

In view of the foregoing, Applicant respectfully requests that the rejection under 35 U.S.C. §103 be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: August 18, 2008

Respectfully submitted,

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